IN THE CLAIMS

Please **cancel** Claims 1-6, 8-13, 17 and 22-25, **amend** Claims 15-18, 21 and 27, and **add** Claims 28-35 as indicated:

1-14. (cancelled)

15. (currently amended) A hard disk drive coupled [[storage device connected]] to a host system, said [[storage device]] hard disk drive comprising at least one driver in an interface section of said [[storage device]] hard disk drive, said at least one driver capable of transmitting to the host system multiple data signals via multiple data signal lines and at least one control signal via at least one control signal line, said multiple data signal lines and said at least one control signal line being allocated in parallel, and said at least one driver capable of sending said data signals with a variable data signal slew rate and said at least one control signal with a variable control signal slew rate, said data signal slew rate having been set smaller than said control signal slew rate by the host system, ~~wherein a transition time of said data signal between a first reference data voltage and a second reference data voltage is longer than a transition time of said control signal between a first reference control voltage and a second reference control voltage by at least 2 nanoseconds.~~ wherein said variable control signal slew rate is determined by an error rate measured in the hard disk drive using Error Correction Codes (ECC), and wherein said variable control signal slew rate is further determined by whether said hard disk drive is coupled to said host system by a cable having 40 or 80 wires, wherein a cable having 80 wires includes grounding lines allocated between wires in the cable to reduce cross-talk noise, and wherein the variable control signal slew rate is set lower if the cable has 80 wires rather than 40 wires.

16. (currently amended) The [[storage device]] hard disk drive according to claim 15, wherein said ~~storage device, being one of at least one storage devices connected to the host system, further comprises a table correlating a quantity of said at least one storage devices to optimum values of said data signal slew rate and said control signal slew rate, and wherein said at least, one driver transmits said multiple data signals and said at least one control signal at said~~

~~optimum values~~ hard disk drive contains a table stored in an ATA Interface Circuit (ATAIFC) in the hard disk drive, wherein the table contains an optimum value of said control signal slew rate, said optimum value being dependent on said error rate measured in the hard disk drive using Error Correction Codes (ECC).

17. (cancelled)

18. (currently amended) The [[storage device]] hard disk drive according to claim 15, wherein said control signal is a strobe signal conforming to AT Attachment (ATA) Specifications.

19. (original) The storage device according to claim 15, wherein said control signal is a strobe signal conforming to ATA Packet Interface (ATAPI) Specifications.

20. (canceled)

21. (currently amended) A computer system comprising:

a host system;

a [[storage device]] hard disk drive;

a cable for connecting [[said]] a host system interface and ~~said storage device~~ a hard disk drive interface, said cable comprising multiple data signal lines and at least one control signal line allocated in parallel;

at least one driver in said host system and at least one driver in said [[storage device]] hard disk drive, each said at least one driver in said host system and each said at least one driver in said [[storage device]] hard disk drive being capable of generating a data signal and a control signal, each said data signal having a variable data signal slew rate and each said control signal having a variable control signal slew rate; and

a table containing an optimum value of said control signal slew rate, said optimum value being dependent on a quantity of hard disk drives connected to said host system and an error rate measured in the hard disk drives using Error Correction Codes (ECC), wherein said host system

sets said optimum value of said control signal slew rate in said control driver upon said host system determining said quantity of hard disk drives and said error rate in the hard disk drives.

~~wherein said host system sets said variable data signal slew rate smaller than said variable control signal slew rate, wherein a transition time of said data signal between a first reference data voltage and a second reference data voltage is longer than a transition time of said control signal between a first reference control voltage and a second reference control voltage by at least 2 nanoseconds.~~

22-26. (cancelled)

27. (currently amended) A data transfer system comprising:

a plurality of data lines for transferring data signals and at least one control line for transferring a control signal, said plurality of data lines and said at least one control line being allocated in parallel;

a data driver connected to at least one of said plurality of data lines;

a control driver connected to at least one of said at least one control line;

a host system, coupled to send and receive said data signals and said control signal to and from at least one [[storage device]] hard disk drive, said host system being capable of dynamically adjusting ~~setting a data signal slew rate and~~ a control signal slew rate [[Such]] such that [[said]] a data signal slew rate is smaller than said control signal slew rate, wherein a setup time for said data signals is shortened, and wherein cross-talk in said data lines remains low due to said data signal slew rate remaining small; and

a table containing an optimum value of said control signal slew rate, said optimum value being dependent on a quantity of [[devices]] hard disk drives connected to said host system[[,]] and an error rate measured in the hard disk drives using Error Correction Codes (ECC), wherein said host system sets said optimum value of said control signal slew rate in said control driver upon said host system determining said quantity of [[devices]] hard disk drives and said error rate in the hard disk drives.

28. (new) The data transfer system of claim 27, wherein the table is stored in an ATA Interface Circuit (ATAIFC) in the hard disk drive.

29. (new) The data transfer system of claim 27, wherein the table is stored in an AT Controller (ATC) in the host system.

30. (new) The data transfer system of claim 27, wherein the optimum value for the control signal slew rate is further dependent on whether a standard hard disk drive (HDD) cable connecting the host system to the hard disk drive has 40 or 80 wires, wherein a HDD cable having 80 wires includes grounding lines allocated between wires in the cable to reduce cross-talk noise, and wherein the data signal slew rate is set higher if the HDD cable has 80 wires rather than 40 wires.

31. (new) The data transfer system of claim 27, wherein the control signal slew rate is controlled by a Driver/Receiver Unit (DRU), wherein the DRU comprises:

means for inputting a Slew Rate Controller (SRC) signal to a plurality of switches, wherein each switch is turned to a first or second position according to a bit in the SRC signal;

a separate Delay Circuit (DLC) coupled to each of the switches;

a plurality of stage inverters, wherein a separate stage inverter is coupled to each of the DLCs;

means for inputting a data signal to a first stage inverter of the plurality of stage inverters; and

in the plurality of stage inverters, means for coupling an output of an upstream stage inverter to an output of a downstream stage inverter, wherein each stage inverter either adds or does not add a lower slew rate to the data signal according to a position of the switch coupled to each stage inverter, and wherein an output of a last downstream stage inverter of the plurality of stage inverters is the data signal having an adjusted slew rate that is a result of a total number of the plurality of stage inverters that have been enabled by the switches to lower a slew rate of the data signal.

32. (new) The computer system of claim 21, wherein the table is stored in an ATA Interface Circuit (ATAIFC) in the hard disk drive.

33. (new) The computer system of claim 21, wherein the table is stored in an AT Controller (ATC) in the host system.

34. (new) The computer system of claim 21, wherein the optimum value for the control signal slew rate is further dependent on whether a cable connecting the host system to the hard disk drive has 40 or 80 wires, wherein a cable having 80 wires includes grounding lines allocated between wires in the cable to reduce cross-talk noise, and wherein the data signal slew rate is set higher if the cable has 80 wires rather than 40 wires.

35. (new) The computer system of claim 21, wherein the control signal slew rate is controlled by a Driver/Receiver Unit (DRU), wherein the DRU comprises:

means for inputting a Slew Rate Controller (SRC) signal to a plurality of switches, wherein each switch is turned to a first or second position according to a bit in the SRC signal;

a separate Delay Circuit (DLC) coupled to each of the switches;

a plurality of stage inverters, wherein a separate stage inverter is coupled to each of the DLCs;

means for inputting a data signal to a first stage inverter of the plurality of stage inverters; and

in the plurality of stage inverters, means for coupling an output of an upstream stage inverter to an output of a downstream stage inverter, wherein each stage inverter either adds or does not add a lower slew rate to the data signal according to a position of the switch coupled to each stage inverter, and wherein an output of a last downstream stage inverter of the plurality of stage inverters is the data signal having an adjusted slew rate that is a result of a total number of the plurality of stage inverters that have been enabled by the switches to lower a slew rate of the data signal.